courtesy to the Examiner, Applicant lists below the references that were cited in each search report and when the references were cited in the present application. A Supplemental Information Disclosure Statement is attached to cite any art from the search reports that has not yet been brought to the Examiner's attention. Applicant will forward copies of the search reports when they become available to Applicant.

PCT/US 95/16984 Search Report dated 6/14/96:

US 5,280,594	cited 2/19/99
"Hyper Page Mode DRAM", 8029 Electronic Engineering, pgs. 47-48	cited 10/31/97
Bursky, Dave, "Novel I/O Options...", Electronic Design, 41	cited 10/31/97
Gowni, Shiva, "Synchronous Cache RAM", IEEE Custom Int. Cir. Conf.	cited 10/31/97

PCT/US 95/16656 Search Report dated 9/18/96:

US 4,984,217	cited herewith

Double Patenting Rejection

In § 4 of the Office Action, claims 59-60 were provisionally rejected (under the judicially created doctrine of obviousness-type double patenting) as being unpatentable over claim 36 of co-pending U.S. Application Serial No. 08/984,563. In § 5 of the Office Action, claim 61 was provisionally rejected (under the judicially created doctrine of obviousness-type double patenting) as being unpatentable over claim 59 of co-pending U.S. Application Serial No. 08/984,561.

Co-pending U.S. Patent Application Serial Nos. 08/984,563 and 08/984,561 have not yet received any final indication of allowed claims. The Applicant requests that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending applications to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicant will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant

application.

Claim Objection

In § 6 of the Office Action, claim 61 was objected to because of informalities. Claim 61 reads as follows:

> A method for accessing several different locations in an asynchronously-accessible memory device, comprising:
>
> selecting a pipeline mode of operation;
>
> providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation;
>
> switching modes to the burst mode of operation;
>
> providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation; and
>
> while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.

The Applicant wishes to note that each of the elements in a method claim are not necessarily limited to execution in the order listed, unless the sequence itself is claimed. See § 38 "Landis On Mechanics of Patent Claim Drafting", Robert C. Faber, 4th Ed. Thus, to answer the first concern expressed, "providing a new external address" occurs "while in a burst mode", and not in the pipeline mode. Respecting the second observation, in the burst mode "at least one subsequent internal address" is generated and patterned after the "initial external address associated with ... the ... memory device in the pipelined mode". It is hoped that these comments resolve the Examiner's concerns, such that claim 61 is now in condition for allowance. Of course, the Applicant stands ready to offer further explanation as needed.

§102 Rejection of the Claims

In § 8 of the Office Action, claims 1-9, 33-35, 46, 48-50, 59-61 and 63-64 were rejected under 35 U.S.C. § 102(e) as being anticipated by Manning (U.S. Pat. No. 5,610,864). The MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the

... claim." *See* M.P.E.P. § 2131. Thus, the Applicant asserts that the Office has failed to show that Manning discusses the identical invention claimed in the instant application, and respectfully traverses this rejection.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in another Office Action mailed to the Applicant on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and *pipelined* modes of operation, as claimed in claims 1, 33, 35, 46, 50, 60, 61, 63, and 64? The Applicant also respectfully draws attention to a statement in the instant Office Action that claim 1 reads on "switching between standard fast page mode (non-EDO) and burst mode". The Applicant's representative was unable to find any portion of Manning to support the idea that fast page mode is the same as a pipelined mode, and requests that such support for this proposition be designated with more specificity.

Second, the Office Action has failed to produce a *prima facie* case of anticipation. The only references offered to support the assertion that Manning "discloses the invention as claimed" with respect to claim 1 are: Fig.1, Ref. 40; col. 5, lines 41-50; col. 6, lines 14-34; and col 7, lines 43-54). Fig. 1, Ref. 40 is a block "mode register", with no indication regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 41-50 discuss the possibility of using a pipelined architecture as an *alternative* to burst operation, but not as enabling switching between pipeline or burst operations, on-the-fly, within the *same* memory, as disclosed by the applicant. Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Again, Manning gives no support whatever to the idea that a pipelined mode of operation is the same as a fast page mode. Thus, Manning never discusses the ability to *select* between burst and pipelined modes of operation, as claimed by the Applicant in independent claim 1, as well as in independent claims 33, 46, 50, 59-61, 63, and 64, and all of the claims which depend from them.

Third, as mentioned in two previous responses to Office Actions in this matter, the Applicant cannot find where Manning discusses that these modes are interchangeable, or

combinable, such that the term "fast page pipeline" proffered in the Office Action is defined. The Applicant still fails to understand the meaning of this particular phrase, and looks to the Office for a more detailed explanation. Otherwise, the Office Action assertion that "Manning discloses mode circuitry to select between fast page pipeline and burst; and circuitry operable in either the burst mode or the pipelined mode coupled to the mode selection circuitry and configured to select between the two modes." is simply not supported by any of the teachings of Manning.

Fourth, the Applicant's representative has also reviewed the Rossini reference mentioned in the Office Action at § 9. It should be noted that Rossini issued on June 7, 1995, which is less than one year before the instant application was filed (on May 20, 1996). The Applicant reserves the right to file a Petition under 37 C.F.R. § 1.131 to swear behind the Rossini reference, if necessary. Moreover, Rossini merely reveals the ability to use a cache controller with various SRAM types ("standard", "burst", or "pipelined burst"). Selecting between "burst and burst pipeline [modes of operation]" within the same memory is not disclosed, as asserted in the Office Action.

In short, what is discussed by Manning and Rossini is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection is improper. Reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

CONCLUSION

The Applicant's representative has reviewed the other art made of record by the Office, but believes that the cited art is more pertinent to the instant application. Thus, the Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested.

The Examiner is invited to telephone Applicant's attorney, Mark Muller, at (210) 308-5677 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 16 day of October, 2001.

Tina Pugh
Name

_____
Signature